## REMARKS

Claims 36-40 and 44-52 were pending in this application. In Decision on Appeal dated November 23, 2010, the rejection of claims 36-40 and 44-52 was affirmed.

Claims 36, 39, 40, 44-49 and 51-52 are hereby amended to more specifically recite aspects. Claims 37-38 and 50 are canceled herein without prejudice or disclaimer. No claim is added herein.

Based on the above Amendment and the following Remarks, Applicants respectfully request withdrawal of the pending rejection.

### Claims as Amended Are Distinguishable over Bergemont and Yamashita

In Decision on Appeal, the rejection of claims 36-40 and 44-52 under 35 U.S.C. § 103(a) over U.S. Patent No. 6,563,731 ("Bergemont") in view of U.S. Patent No. 6,777,758 ("Yamashita") was affirmed. This rejection is overcome in view of the amendment.

Independent claim 36, as amended, recites, in part:

> a shorted transistor for removing electrons from the floating gate, ***the shorted transistor comprising***:
>
> a p- doped substrate including a second n-well, a second drain within the second n-well, and a second source within the second n-well;
>
> a second layer of gate oxide above said first n- well;
>
> a second polysilicon floating gate above said second layer of gate oxide, the second polysilicon floating gate connected to the first polysilicon floating gate; and
>
> ***a conductor connecting the second drain and the second source***, a number of electrons removed from the second polysilicon floating gate increased responsive to increase in voltage at the second drain or the second source.

Per claim 36, a pFET synapse transistor includes a shorted transistor. The shorted transistor removes electrons from the floating gate. The shorted transistor comprises a p-doped substrate, a second layer of gate oxide, a second polysilicon floating gate and a conductor. The p- doped substrate includes a second a second n-well, a second drain within the second n-well, and a second source within the second n-well. The conductor connects the second drain and the second source. The number of electrons removed from the second polysilicon floating gate is increased when the voltage is increased at the second drain or the second source.

Bergemont and Yamashita fail to disclose the feature of "the shorted transistor comprising . . . a conductor connecting the second drain and the second source," as recited in claim 36, as amended. A cell (e.g., cell 603) in Bergemont includes a floating gate (e.g., gate 610) spanning across n-well (e.g., well 607) and P region (e.g., region 618). See 5:59-6:2; and FIG. 6. As clearly shown in FIG. 6 of Bergemont, a cell in Bergemont does not include any shorted transistor or components having a conductor connect drain and the source.

Nor does Yamashita disclose such feature. Yamashita was cited in the Examiner's Answer and Decision on Appeal for allegedly disclosing a well contact terminal. Yamashita discloses nothing about a shorted transistor having its drain and source connected via a conductor.

Therefore, claim 36, as amended, is patentably distinguishable over Bergemont and Yamashita for reciting the feature of "the shorted transistor comprising . . . a conductor connecting the second drain and the second source . . . ."

Claims 39 and 40 depend from claim 36, and therefore, the same arguments set forth above for claim 36 are applicable to claims 39 and 40.

Independent claims 44-48 also recite the feature of "the shorted transistor comprising . . . a conductor connecting the second drain and the second source . . . ." Therefore, claims 44-48 and claim 49 (depending from claim 48) are also patentably distinguishable over Bergemont and Yamashita for reciting this feature.

Based on the above Amendment and the following Remarks, Applicants respectfully request withdraw of the rejection.

**Conclusion**

Favorable action is solicited.

Respectfully submitted,

Dated: January 18, 2011

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